

AIN SHAMS UNIVERSITY FACULTY OF ENGINEERING

Project 3 Report

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Program: Computer Engineering and Software Systems (CESS).

***1.Introduction:***

In the previous part of the project (logical synthesis) we have been drive the final sdetj\_scan.vst file of our chip, in this part of the project we would make the physical synthesis (placement and routing) for our chip with the following alliance cad tools:

•**ocp:** Standard Cell Placer.

• **nero:** Over-Cell Router.

• **cougar:** Symbolic Netlist Extractor.

• **lvx:** Netlist comparator.

• **graal:** Symbolic layout editor.

• **druc:** Symbolic Design-rule checker.

• **Ring:** Pad ring router.

• **s2r :** Symbolic-to-Real layout converter.

• **dreal :** Real layout editor.

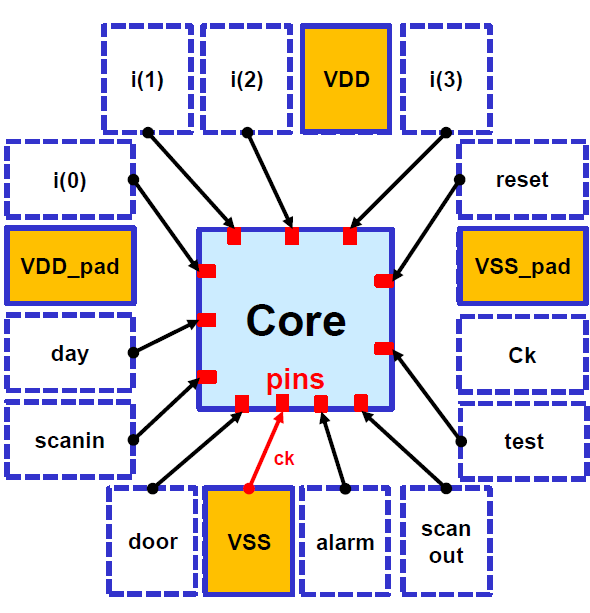
During physical synthesis, we are going to use the following technology parameter files:

• **techno/techno-symb.rds :** the Symbolic technology parameters file.

• **techno/techno-035.rds :** A generic 0.35 micron technology parameters file.

***2.Floor planning:***

Before starting physical synthesis, we must first construct the chip floor planning:

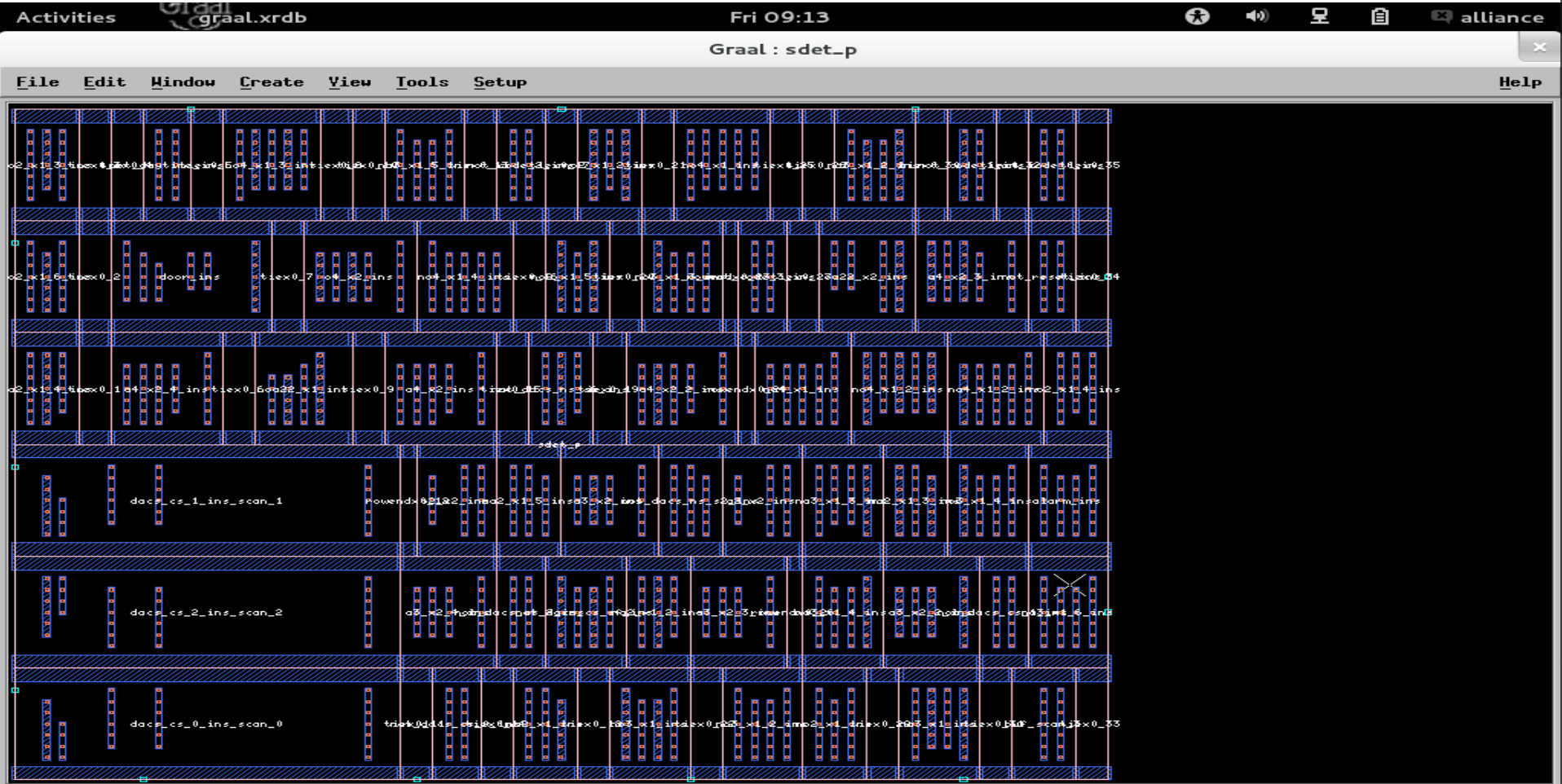


***3.Placement:***

To launch placement, we will use the **ocp** tool with this command: 

The **–ioc** option permits to specify a placement for external connectors (pins) described in a .ioc file. The –ring option permits to automatically place the connectors for the ring pad placement tool. In our case, the **MBK\_IN\_LO** variable should be set to **vst**. The last argument is the name of the **.ap** resulting symbolic layout file. The **MBK\_OUT\_PH** variable should be set to **ap**.

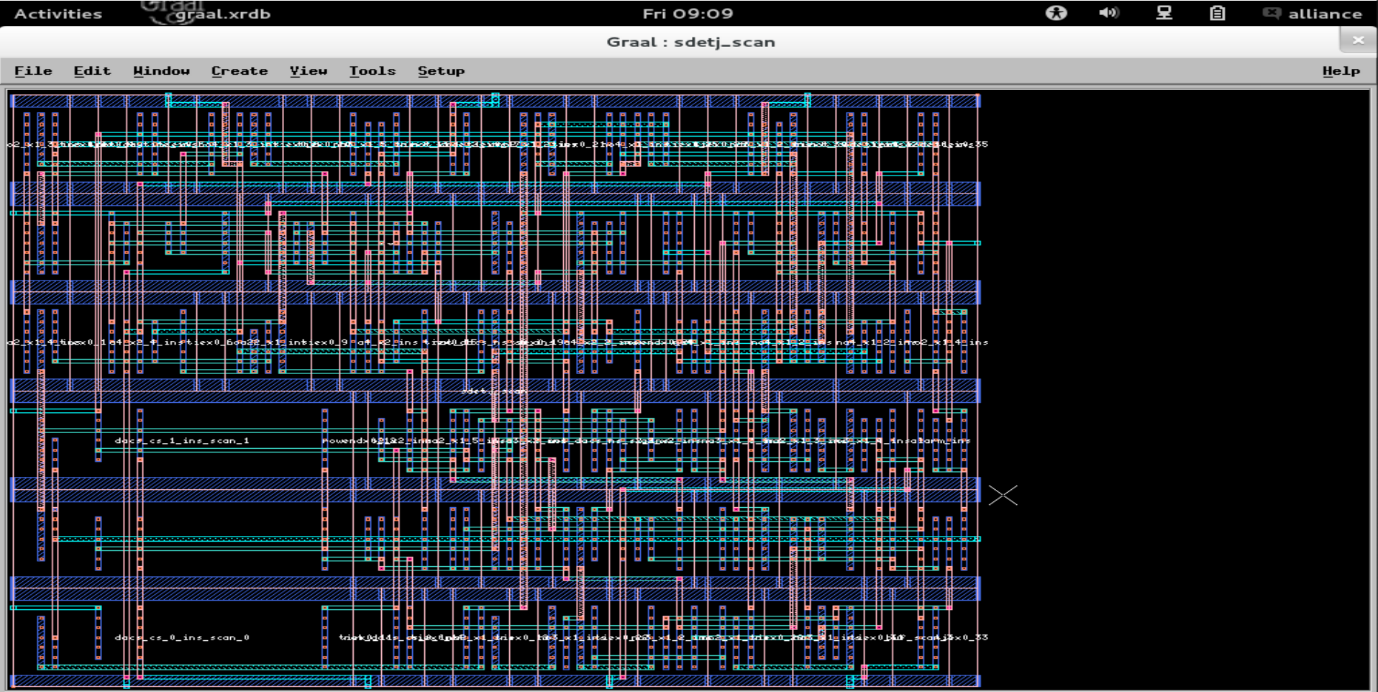
In order to review the resulting placement, the symbolic layout editor **graal** can be used:



***4.Routing:***

Routing the placed cells is done by using **nero** in the following way: 

**The final layout must have the same file name as the netlist**, but with different extensions. This will be required by the **ring** pad placement and routing tool.

The layout editor tool **graal** can be then used to inspect the output layout:

***5.Post-Layout Verification:***

Post-layout verification is composed of two steps: electrical and physical. Electrical verification checks that the extracted netlist is exactly the same as the gate-level netlist (LVS), while physical verification checks if there are design-rule errors in the generated layout (DRC).

***5.1.Layout-vs-Schematics (LVS):***

Netlist comparison is done on two steps; first the netlist is extracted using the **cougar** tool. The original netlist is in **vst** format. We’ll have the extracted netlist in **al** format, in order not to overwrite files. This can be achieved by setting the **MBK\_OUT\_LO** to **al**. Also, we should set the technology file environment variable **RDS\_TECHNO\_NAME** to the real technology parameter file **techno/techno-035.rds**.

Netlist extraction is then performed using the command: 

This is followed by netlist comparison using the command: 

***5.2.Design-Rule Checking (DRC):***

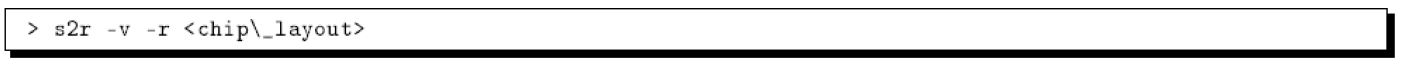
Design-rule checking can be done using two methods:

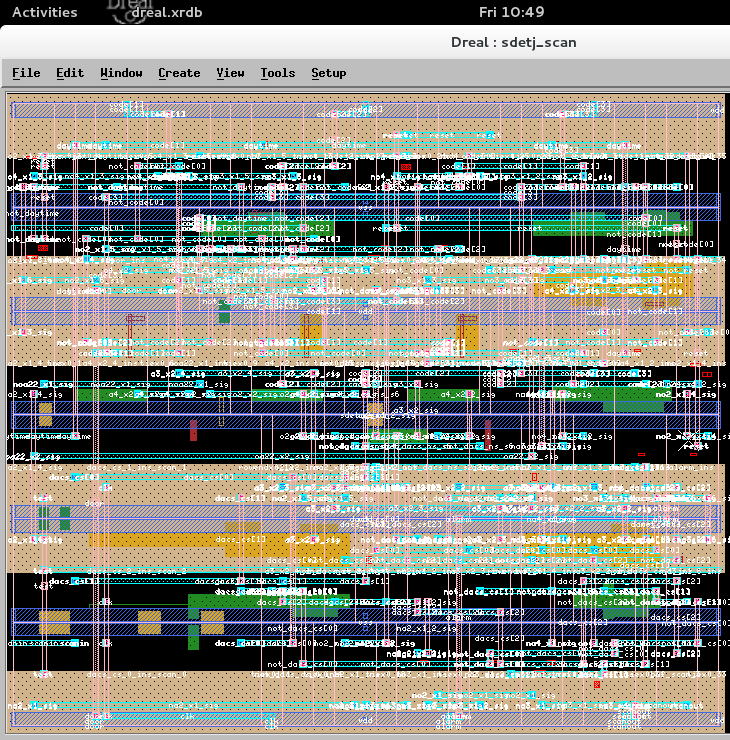
• Inside the layout editor tool **graal**, open the generated layout. Select from the menus Tools->Druc, then select the whole layout using the mouse.

• Using the **druc** design rule checker. In order to check symbolic rules, the technology file environment variable **RDS\_TECHNO\_NAME** should be set to the symbolic technology parameter file **techno/techno-symb.rds**. 

In this project we will use the second method.

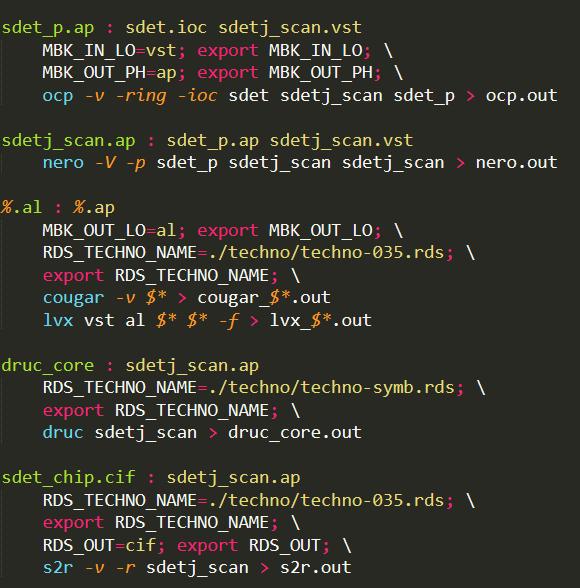
***6.Symbolic-to-Real Conversion:***

Finally, the generated symbolic layout should be converted to a real fabrication technology. We’ll use a standard cif output format for the real layout. The **RDS\_OUT** variable must be set to **cif**. Technology is specified by setting the **RDS\_TECHNO\_NAME** to the real technology parameter file **techno/techno-035.rds**. Conversion is then done using the command: 

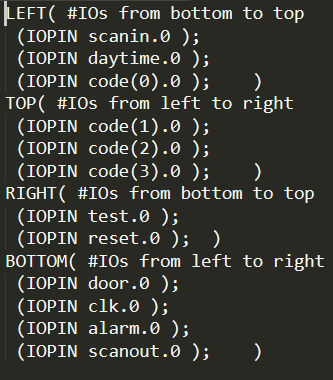
view this file using the **dreal** real layout viewer. 

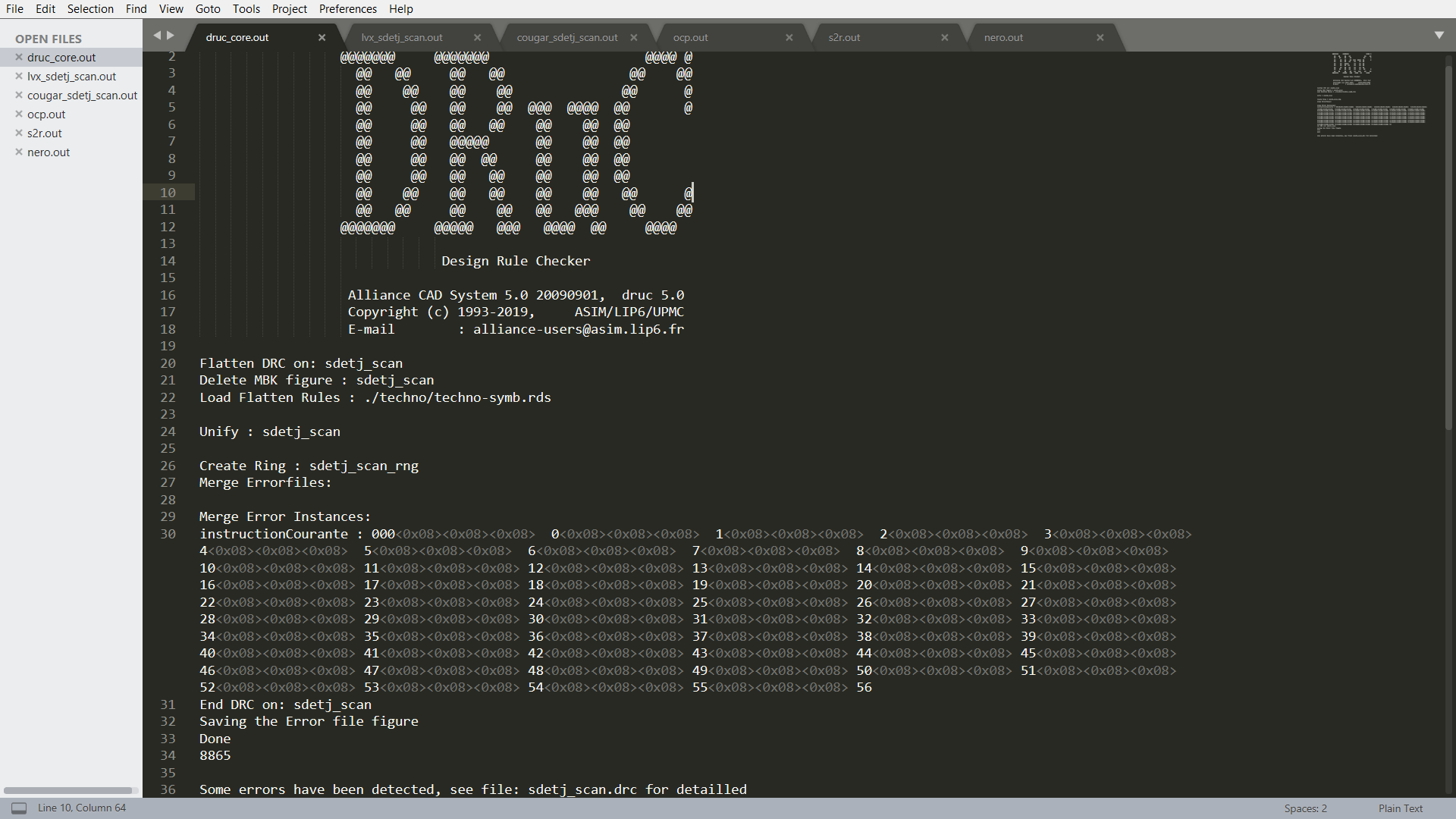
***7.Appendix:***

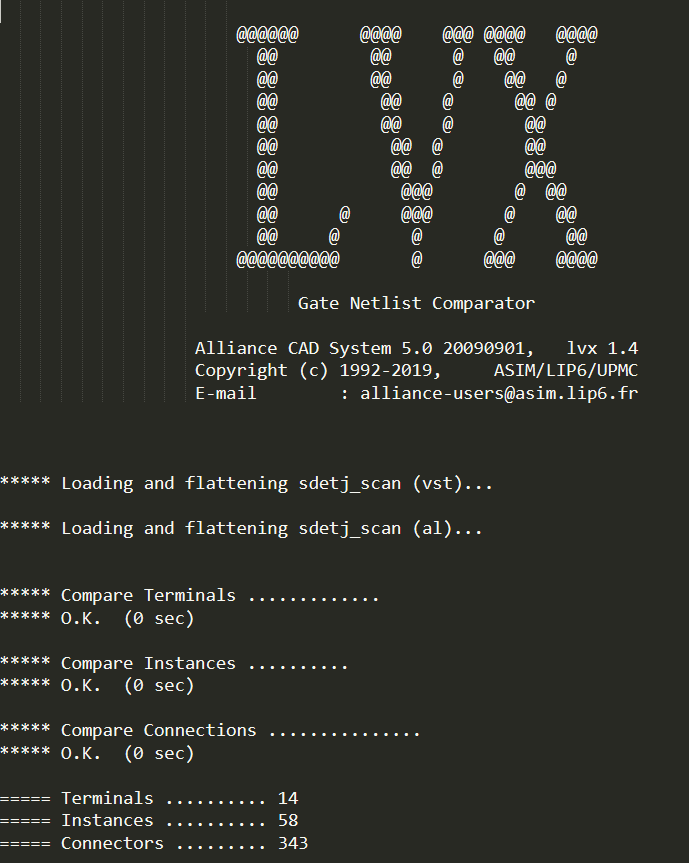
Make file:



.ioc file:



DRUC output: 

LVX output: 

Coujar output: 